abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Election

In response to the Restriction Requirement listing Inventions I and II, Applicants elect without traverse to prosecute the claims 1-17, 26-40, and 49-52 of Invention I.

Amendments

In the Specification:

Please substitute pending paragraph 0050 with the following paragraph 0050:

FIGS. 32A (comprising FIGS. 32A-1, 32A-2, 32A-3, and 32A-4) and 32B (comprising FIGS. 32B-1, 32B-2, and 32B-3) show further detail of a receiver channel, according to an example differential receiver channel embodiment of the present invention.

Please substitute pending paragraph 0274 with the following paragraph 0274:

The present invention is applicable to any 802.11 WLAN receiver implementations, including differential receiver channel configurations. FIGS. 32A and 32B show further details of receiver channel 1700, according to an example differential

receiver channel embodiment of the present invention. FIGS. 32A and 32B incorporate embodiments of feedback loop 1900 and automatic gain control, according to embodiments of the present invention. FIG. 32A comprises FIGS. 32A-1, 32A-2, 32A-3, 32A-4, and FIG. 32B comprises FIGS. 32B-1, 32B-2, and 32B-3. FIGS. 32A-1, 32A-2, 32A-3, and 32A-4 show a first portion of receiver channel 1700, including second AGC amplifier 1604, first amplifier/filter section 1608, and multiplier 1702. FIGS. 32B-1, 32B-2, and 32B-3 show a second portion of receiver channel 1700, including first AGC amplifier 1610 and second optional amplifier/filter section 1612. An antenna and down-converter are not shown in the portions of receiver channel 1700 shown in FIGS. 32A-1, 32A-2, 32A-3, 32A-4, 32B-1, 32B-2, and 32B-3. FIG. 30 shows a differential UFD module that may be used as a differential down-converter in down-converter 1606 shown in FIGS. 16 and 17, according to embodiments of the present invention. The invention is also applicable to other types of differential down-converters.

A2 Cont.

Please substitute pending paragraph 0275 with the following paragraph 0275:

As shown in FIG. 32A-3, an input differential signal 3210 is received by second AGC amplifier 1604. Input differential signal 3210 is a differential signal, and second AGC amplifier 1604 is a differential AGC amplifier. Input differential signal 3210 may be a differential version of a received RF signal or IF signal, for example.

A3

Please substitute pending paragraph 0281 with the following paragraph 0281:

As stated above, receiver channel 1700 shown in FIGS. 32A and 32B include automatic gain control features of the present invention. These features are more fully described in section 4.4. As shown in FIG. 32A-1, multiplier 1702 receives first AGC signal 1704 and generates second AGC signal 1706. Second AGC signal 1706 is input to second AGC amplifier 1604 in FIG. 32A-3. First AGC signal 1704 is input to first AGC amplifier 1610 in FIG. 32B-1. Multiplier 1702 is shown in FIG. 32A-1 as an operational amplifier implemented in a non-inverting configuration, but may be implemented in alternative configurations. The AGC signals for second AGC amplifier 1604 and first AGC amplifier 1610 are based upon a single AGC signal source that generates first AGC signal 1704. Furthermore, multiplier 1702 allows for faster gain control in second AGC amplifier 1604 than in first AGC amplifier 1610, by amplifying first AGC signal 1704 to generate a greater amplitude second AGC signal 1706.

Please substitute pending paragraph 0282 with the following paragraph 0282:

In FIG. 32B-1, first AGC amplifier 1610 receives receiver channel differential signal 3212, and outputs an amplified differential signal.

Please substitute pending paragraph 0285 with the following paragraph 0285:

First amplifier 1902d provides for gain/attenuation in the feedback loop. First amplifier 1902d is shown in FIG. 32B-3 as a resistor voltage-divider circuit. First amplifier 1902d receives and attenuates output signal 1628 according to the voltage divider, and outputs an attenuated output signal 1920d.

Please substitute pending paragraph 0286 with the following paragraph 0286:

Integrator 1904d provides for a variable frequency response, similarly to that of integrator 1904 shown in FIG. 23. Integrator 1904d receives the two control signals ACQ1 3104 and ACQ2 3102, that control the opening and closing of switches 2308d and 2310d (and switches 2308c and 2310c in integrator 1904c shown in FIGS. 32A-2 and 32A-1) in integrator 1904d of FIGS. 32B-1, 32B-2, and 32B-3, in order to vary the frequency response of feedback loop 1900d.

Please substitute pending paragraph 0288 with the following paragraph 0288:

FIG. 35 shows a first frequency response waveform 3500 resulting when ACQ1 3104 and ACQ2 3102 are both set to high. This setting indicates a short time constant has been selected for integrators 1904a and 1904b in FIGS. 31A-B, or for integrators 1904c and 1904d in FIGS. 32A-1, 32A-2, 32B-1, 32B-2, and 32B-3. As can be seen in

a8 cont.

FIG. 35, a high-pass corner frequency for first frequency response waveform 3500 is located near 2.5 MHz.

Please substitute pending paragraph 0289 with the following paragraph 0289:

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FIG. 36 shows a second frequency response waveform 3600 resulting when ACQ1 3104 is set to a high level and ACQ2 3102 is set to a low level. This setting indicates a medium time constant has been selected for integrators 1904a and 1904b in FIGS. 31A-B, or for integrators 1904c and 1904d in FIGS. 32A-1, 32A-2, 32B-1, 32B-2, and 32B-3. As can be seen in FIG. 36, a high-pass corner frequency for second frequency response waveform 3600 is located near 269 KHz.

Please substitute pending paragraph 0290 with the following paragraph 0290:

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FIG. 37 shows a third frequency response waveform 3700 resulting when ACQ1 3104 and ACQ2 3102 are both set to low levels. This setting indicates a long time constant has been selected for integrators 1904a and 1904b in FIGS. 31A-B, or for integrators 1904c and 1904d in FIGS. 32A-1, 32A-2, 32B-1, 32B-2, and 32B-3. As can be seen in FIG. 37, a high-pass corner frequency for third frequency response waveform 3700 is located near 21.6 KHz.

Please substitute pending paragraph 0297 with the following paragraph 0297:

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Receiver channel 1700 as shown in FIGS. 32A and 32B provides for gain, filtering, and DC offset voltage reduction for input differential signal 3210. Output signal 1628, shown in FIG. 32B-3, is the output signal for receiver channel 1700. As can be seen in the embodiment of FIG. 38, output signal 1628 is an approximately 1 MHz information signal.

In the Claims:

Please cancel claims 18-25 and 41-48 without prejudice or disclaimer.